9309

MSI DUAL FOUR-INPUT MULTIPLEXER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9309 is a monolithic, high speed, dual four-input digital multiplexer circuit, constructed with the Fairchild Planar* epitaxial process. It consists of two multiplexing circuits with common input select logic, each circuit contains four inputs and fully buffered complementary outputs. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTμL for high speed, high fanout operation and is compatible with all other members of the CCSL family of digital integrated circuits.

FEATURES

- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, TTμL, AND MSI FAMILIES (CCSL).**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS.**

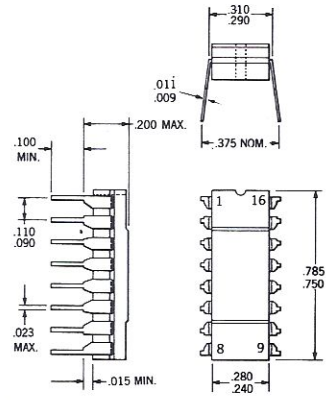
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs (Output high)	−0.5 V to +V_{CC} value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5 V
Input Current (DC) (See Note 1)	−30 mA to +5 mA
Current into Output (Output low)	+30 mA

Note 1—either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ORDER INFORMATION — Specify U6B9309XXX for 16-pin Dual In-Line package or U3L9309XXX for 16-pin Flatpak, where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

Fig. 1

FLAT PACKAGE

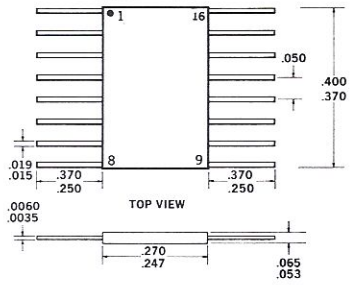
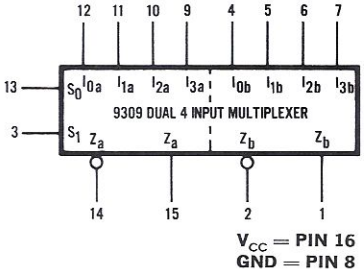


Fig. 2

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Fig. 3

*Planar is a patented Fairchild process.

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MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

TRUTH TABLES

INPUTS						OUTPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{a0}	I_{a1}	I_{a2}	I_{a3}	Z_a	$\overline{Z}_a$	I_{b0}	I_{b1}	I_{b2}	I_{b3}	Z_b	$\overline{Z}_b$
L	L	L	X	X	X	L	H	L	X	X	X	L	H
L	L	H	X	X	X	H	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H	X	L	X	X	L	H
H	L	X	H	X	X	H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L	X	X	H	X	H	L
H	H	X	X	X	L	L	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = don't care

LOADING RULES

(1 U.L. = 1 TTμL gate input load)

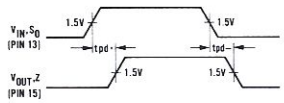
INPUTS	LOADING
I_{a0}, I_{a1}, I_{a2}, I_{a3}, I_{b0}, I_{b1}, I_{b2}, I_{b3}, S_0, S_1	1 U.L.
OUTPUTS	**FANOUT**
Z_a, Z_b	10 U.L.
$\overline{Z}_a$, $\overline{Z}_b$	9 U.L.

A.C. CHARACTERISTICS

All delays are measured with V_{CC} = 5.0 V applied to pin 16 and pin 8 grounded. The active input is driven by a 9002 TTμL gate with the output loaded with 15 pf. All outputs are loaded with 15 pf.

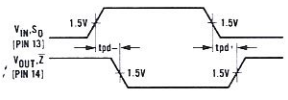
t_{pd}; S_0 to Z_a

CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}



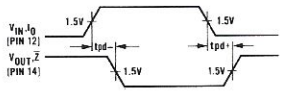
t_{pd}; S_0 to $\overline{Z}_a$

CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}

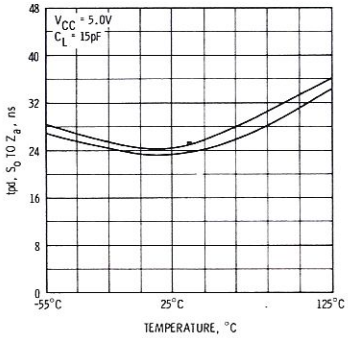


t_{pd}; I_{a0} to $\overline{Z}_a$

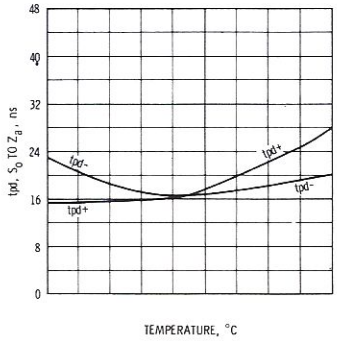
CONDITIONS
Pin 3, 13 = GND.



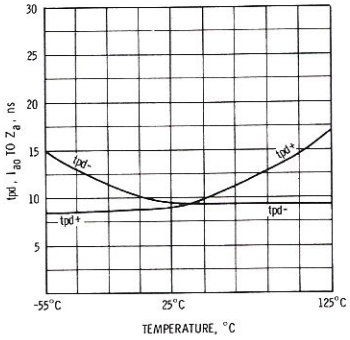
TYPICAL PROPAGATION DELAYS VERSUS TEMPERATURE, S_0 to Z_a



TYPICAL PROPAGATION DELAYS VERSUS TEMPERATURE, S_0 to Z_a



TYPICAL PROPAGATION DELAYS VERSUS TEMPERATURE, I_{a0} to Z_a



ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part No. UXX930951X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4$ mA (Pins 1 & 15) $I_{OL} = 11.2$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		30	40		40		$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} S_0 to Z_a	Switching Speed				24	32			ns	$V_{CC} = 5.0\ V$, See Figure 5
t_{pd-} S_0 to Z_a	Switching Speed				24	32			ns	

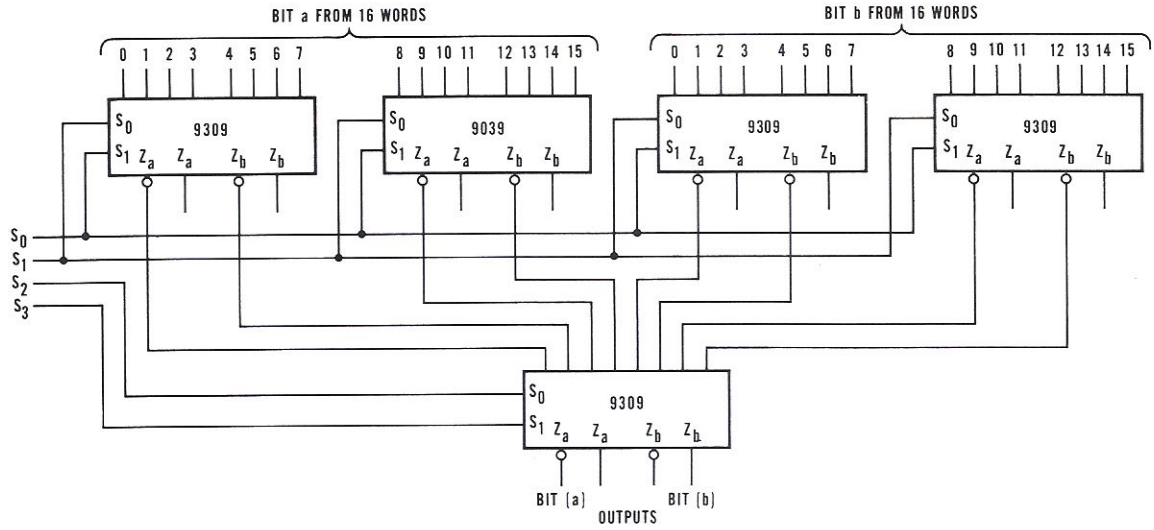
*Pulse tested

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part No. UXX930959X)

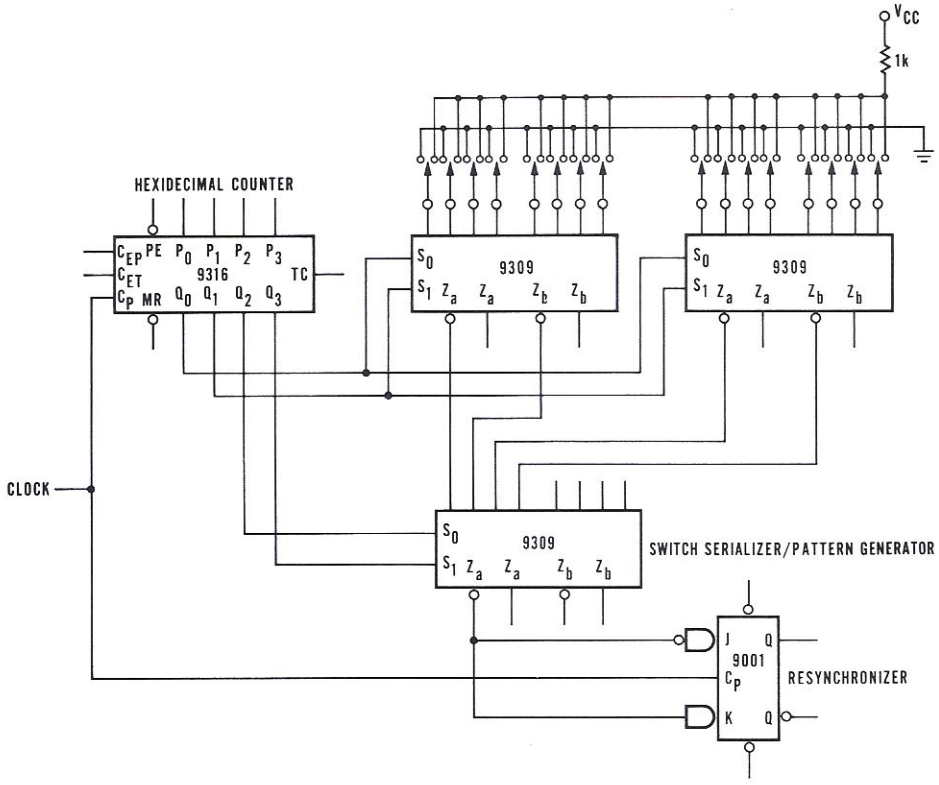
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1$ mA (Pins 1 & 15) $I_{OL} = 12.7$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		30	43		43	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} S_0 to Z_a	Switching Speed				24	32			ns	$V_{CC} = 5.0\ V$, See Figure 5
t_{pd-} S_0 to Z_a	Switching Speed				24	32			ns	

*Pulse tested

APPLICATIONS



A. Five 9309's provide switching of data from sixteen two-bit words onto a two-bit output data buss. The selection of which bit to be transferred is made by the address inputs S_0, S_1, S_2 and S_3.



B. Sixteen-Bit Pattern Generator.

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